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Application Note

# USING LOW-COST 1 MHz PERIPHERALS IN A 2 MHz SYSTEM WITH THE MC68B09 AND THE MC68B09E

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## INTRODUCTION

With the increasing use of HMOS design techniques in VLSI circuits, the maximum speed of these devices is also on the rise. There are 2 MHz, "B," versions of the popular MC6809 and the new MC6809E with external clock. Both the MC68B09 and the MC68B09E feature a 500 nanosecond cycle time. With a 2 MHz E clock, an add immediate instruction takes just 1 microsecond! These fast, efficient processors offer designers the opportunity to use a microprocessor in applications which have been, until now, too slow.

It would appear that the speed increase necessarily carries with it a cost penalty. That is, by increasing the speed of the bus, faster and therefore more expensive memories and peripherals must be used. However, there are ways to manipulate the 2 MHz MPU access time to accommodate slower peripherals and memories.

## MPU ACCESS TIME MANIPULATION

The system clocks on the MC6809 can be delayed (stretched) to allow longer access time for slow memories using the MRDY input pin. Figure 1 shows the timing for this input. The system E and Q clocks are stretched, while E is high and Q is low, in one-quarter bus cycle increments. One quarter cycle of the MC68B09 2 MHz clock is equal to 125 nanoseconds. Since the MC6809E requires an external clock generator, the MRDY signal can be implemented externally for that processor.

A problem arises when stretching the access time for slow memories in that the throughput of the 2 MHz system is reduced markedly because the majority of processor cycles are, in fact, memory accesses. One solution to this problem is a compromise: absorb the cost of fast memories to allow the processor to run all memory cycles at full speed but reduce the speed of the bus for peripheral access. Since many peripherals are accessed only infrequently, this approach incurs minor impact on total throughput.

Unfortunately, slowing the bus cycle to accommodate slow peripherals is not as simple as using slow memories. To begin with, all MC6809 family peripherals require a continuous system clock to function. If the peripherals are specified at 1 MHz, this clock cannot exceed 1 MHz. This requires a separate, 1 MHz peripheral clock. This clock may not be synchronous with the main 2 MHz processor clock. Therefore, the chip enable signals to the peripherals must be delayed until the peripheral clock is low and then meet the chip select ($\overline{CS}$) setup time. In 1 MHz chips, chip select time is 160 nanoseconds before the rising edge of the clock. Some circuits, designed to allow the use of an MC6809 peripheral chip operating at one-half the frequency of the 2 MHz system clock, are described in the following paragraphs.

## USING THE MC68B09 WITH 1 MHz PERIPHERALS

The circuit shown in Figure 2 allows 1 MHz peripherals to run with a 2 MHz MC68B09 system by generating an asynchronous peripheral clock (PCLK). When an access of any 1 MHz peripheral takes place, the 2 MHz system clocks, E and Q, are stretched using the MRDY pin. A state machine then waits until PCLK is low and then chip selects the peripheral 250 nanoseconds before the rising edge of PCLK. This provides proper address setup time at the peripherals before chip selecting them. Clocks E and Q are then released and the data is latched.

Refer to the timing diagram in Figure 3 and note the signal relationships during write and read cycles. Initiation of a

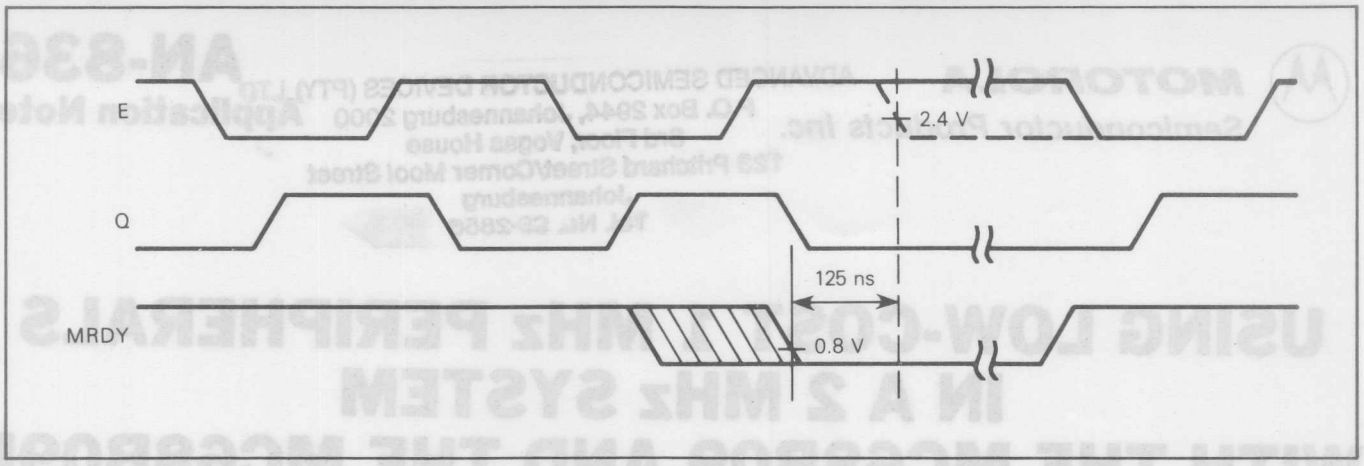


**Figure 1. MC6809 MRDY Timing**

peripheral access cycle causes the address decoding logic to bring the PERAC signal high ①. Signal MRDY is then brought low ②. While MRDY is low, the high E and low Q clocks are inhibited from switching states. Allowing for the address setup time, the peripheral enable (PE) signal is made true in the center of the PCLK low cycle ③.

Signal MRDY is then raised 375 nanoseconds after the rising edge of PCLK allowing E to fall 125 nanoseconds later ④. In addition, if the access is a read, PCLK is stretched 125 nanoseconds past the fall of E ⑤ to ensure valid data from the peripheral. The delay also allows for some inherent skew in the processor MRDY to E falling time. If the access is a write to the peripheral, then E is allowed to fall after PCLK to ensure that the peripheral clocks in valid data.

Note on Figure 3 that peripheral access (PERAC) may become active high either during the low or high cycle of PCLK. If the access occurs during the first quarter of the PCLK cycle, the E need only be stretched for one 2 MHz bus cycle (250 nanoseconds) until PCLK falls. However, if the access occurs during the last three-quarters of the PCLK cycle, then the stretch has to be continued until the next full cycle of PCLK occurs. The best case example, shown in Figure 3, is a short write, where the write PERAC signal occurs before the end of the first quarter cycle of PCLK. The worst case is a long read, where the read PERAC signal occurs during PCLK high.

## MC6809E CLOCK CIRCUIT

Unlike the MC6809, the MC6809E requires an external clock generator to provide the 2 MHz E and Q system clocks. Figure 4 shows a circuit that can generate these clocks. The circuit also generates an internal PCLK signal used to develop the chip select ($\overline{CS}$) output to the peripherals. This output ensures that an addressed peripheral is accessed at the proper time. Two inputs are required by the circuit. These are the MRDY and the PERAC inputs. Input MRDY is used to stretch the E and Q clocks during slow (1 MHz) peripheral access cycles. Input PERAC is used to signal that a slow peripheral access cycle is active.

An 8 MHz oscillator, formed by crystal Y1, related 74LS04 U4 inverters, and resistors R1 and R2, provides the reference frequency. Two 8 MHz outputs, $\overline{4X}$ and 4X are obtained from the oscillator. Output $\overline{4X}$ is used to clock binary counter U7. This counter divides the $\overline{4X}$ clock by 2, 4, and 8 to derive the 4 MHz 2X clock, the 2 MHz 1X clock, and the 1 MHz PCLK, respectively. Clock 2X is routed to flip-flop U3a, where it is divided by 2 to obtain the 2 MHz Q clock output. Clock 1X is routed via gate U6a to provide the 2 MHz E clock output.

At power-up, flip-flop U3a and U3b are used to establish the correct clock E and clock Q phase relationship. However, this synchronization must be delayed until the oscillator has stabilized. An RC network (C1, R3) provides this delay. At power-up, a momentary low level from the RC network clears U3b to hold the U3b output low. In turn, the low U3b output presets U3a to hold the system Q clock output high. Approximately 50 milliseconds after power-up, the RC network output reaches $V_T$ (1.9 V) of inverter U9 and releases U3b so it can be toggled by clock E. As the D input of U3b is tied to +5 V, the next rising edge of clock E toggles the U3b output from low to high. This action releases the U3a preset input so that U3a can be toggled by clock 2X. The next rising edge of clock 2X, and all subsequent rising edges of 2X, switch the U3a system Q clock output to generate the Q waveform. The +5 V at the D input of U3b ensures that the U3b output remains high and does not interfere with U3a after synchronization. Since the system reset delay is 100 milliseconds, the 50 millisecond clock delay does not interfere in any way with system operation.

## MC6809E SLOW MEMORY ACCESS

The MRDY input allows the processor to access slow memories by stretching E and Q. Refer to the timing diagram in Figure 5 and note that when MRDY is pulled low, E is high and Q is low. Refer to Figure 4 and note that these conditions generate a low output at gate U5c. Therefore, a low is present at the input of U2b. The next rising edge of the oscillator 4X clock toggles U2b and causes ENABLE to counter U7 to become inactive, holding E high. The Q clock is also held low by the low clear input to U3a from U2b. Thus, E and Q are stretched as long as MRDY is low. Removing MRDY causes the clocks to be released on the following 4X clock rising edge.

## MC6809E SLOW PERIPHERAL ACCESS

Correct access of slow peripherals dictates synchronization between the processor clock, E, and peripheral clock, PCLK. In this case, PCLK is a continuous square wave one-half the frequency of E. Accesses of the slow peripheral are synchronized by stretching E, thus allowing them to operate at their full rated bus speed. Only the processor is slow and only for that cycle.

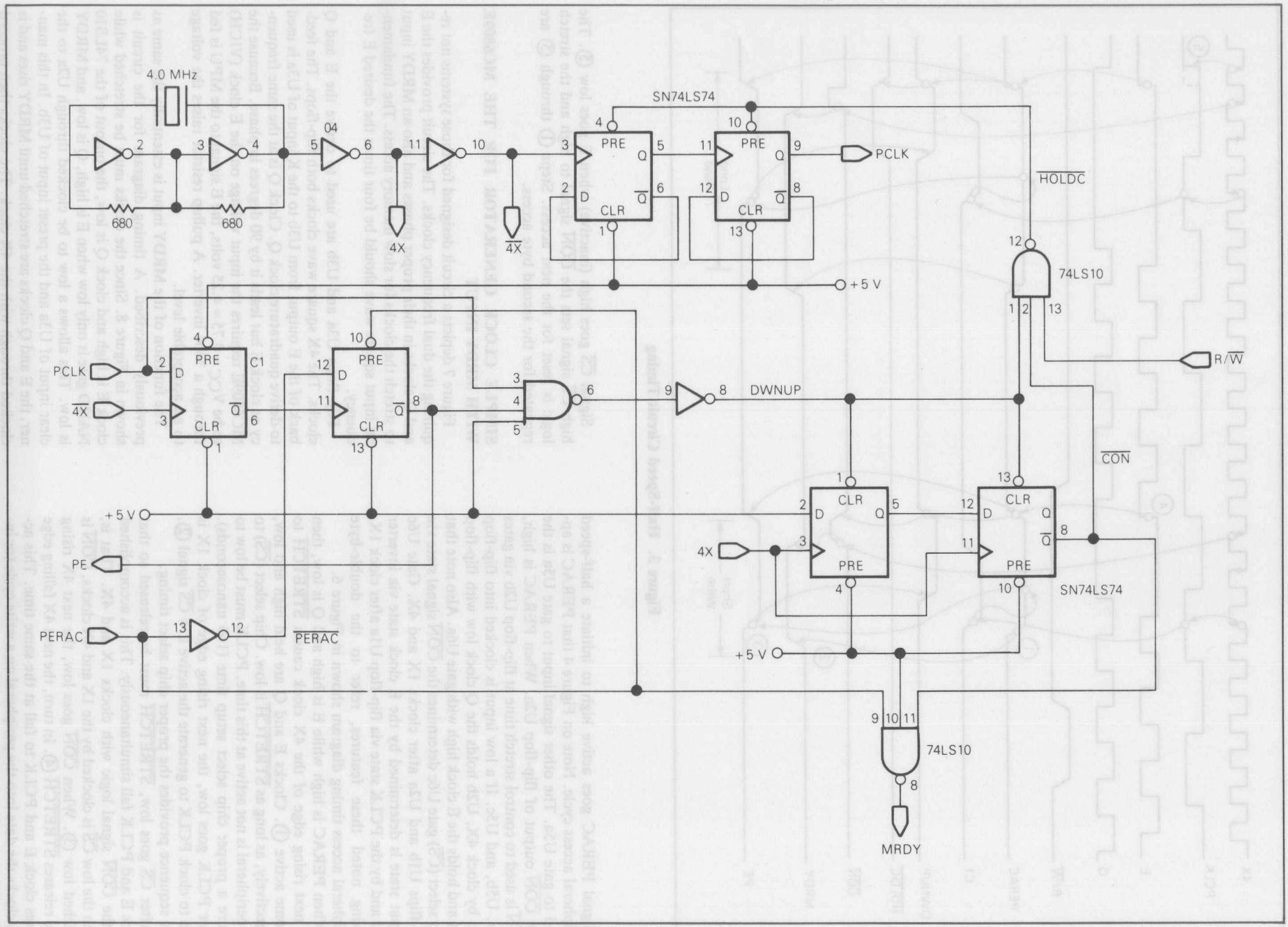


**Figure 2. MC6809 Half-Speed Peripheral Clock Circuit**

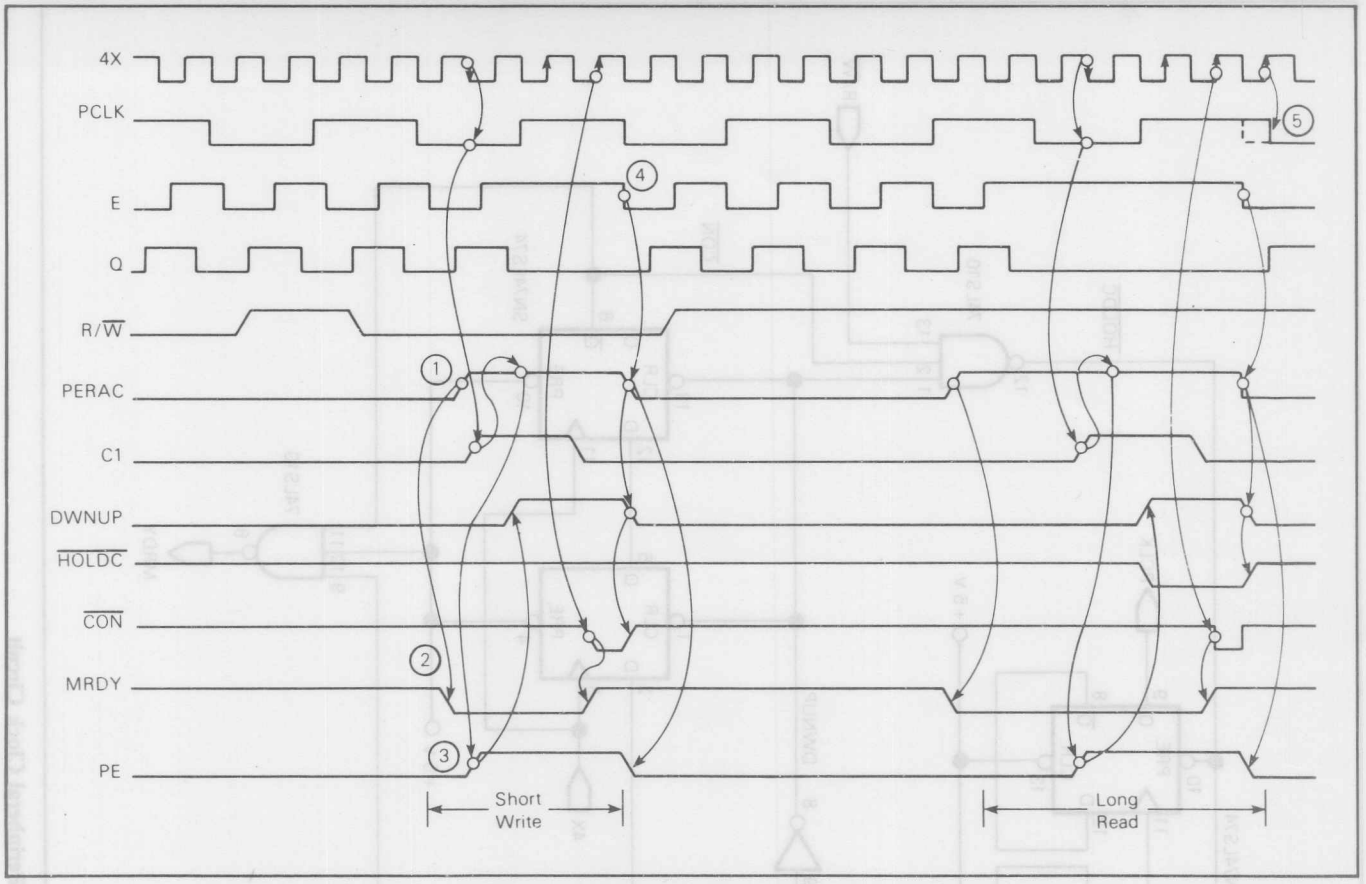


**Figure 3. Half-Speed Circuit Timing**

Signal PERAC goes active high to initiate a half-speed peripheral access cycle. Note on Figure 4 that PERAC is applied to gate U5a. The other signal input to gate U5a is the high $\overline{CON}$ output of flip-flop U2a. When PERAC is high, $\overline{CON}$ is used to control stretch time at flip-flop U2b via gates U5a, U5b, and U5c. If a low input is clocked into flip-flop U2b by clock 4X, U2b holds the Q clock low with flip-flop U3a and holds the E clock high with gate U6a. Also note that chip select ($\overline{CS}$) gate U6c determines the $\overline{CON}$ signal state via flip-flips U1b and U2a after clocks 1X and 4X. Gate U6c output state is determined by the E clock state via inverter U4d and by the PCLK state via flip-flop U1a after clock 1X. Having noted these features, refer to the double-byte peripheral access timing diagram shown in Figure 6.

When PERAC is high while E is high and Q is low, then the next rising edge of the 4X clock causes $\overline{STRETCH}$ to become active ①. Clocks E and Q are held high and low, respectively, as long as $\overline{STRETCH}$ is low. Chip select ($\overline{CS}$) to the peripheral is not active at this time. PCLK must be low to ensure a proper chip select setup time (160 nanoseconds). After PCLK goes low, the next rising edge of clock 1X is used to clock PCLK to generate the active low $\overline{CS}$ signal ②. This sequence provides the proper chip select timing.

After $\overline{CS}$ goes low, $\overline{STRETCH}$ must be released so that clock E and PCLK fall simultaneously. This is accomplished by the $\overline{CON}$ signal logic with clocks 1X and 4X. That is, when the low $\overline{CS}$ is clocked by the 1X and 4X clocks, $\overline{CON}$ is switched low ③. When $\overline{CON}$ goes low, the next 4X rising edge releases $\overline{STRETCH}$ ④. In turn, the next 4X falling edge causes clock E and PCLK to fall at the same time. This action clocks the data into the peripheral on a write cycle (or into the MPU on a read cycle).

Signal $\overline{CS}$ goes high (inactive) when E goes low ⑤. The high $\overline{CS}$ signal sets the $\overline{CON}$ signal to high and the stretch logic is reset for the next access. Steps ① through ⑤ are repeated for the second byte access.

## SIMPLE CLOCK GENERATOR FOR THE MC6809E WITH MRDY INPUT

Figure 7 depicts a circuit designed for those systems not requiring the dual frequency clocks. The circuit provides the E and Q clocks in their proper phases and also an MRDY input to stretch the clocks for slow memory access. The fundamental input square wave should be four times the desired E frequency.

Flip-flops U3a and U3b are used to derive the E and Q clocks. The 4X square wave clocks both flip-flops. The feedback of the E output from U3b to the K input of U3a is used to derive quadrature clock Q. Clock Q is at the same frequency as clock E but leads it by 90 degrees in phase. Because the MC6809E requires the input voltage on the E clock (VICH) to be $V_{CC} - 0.75 = 4.25$ volts, the E signal to the MPU is fed through a 7404 inverter. A pullup resistor raises the voltage to an acceptable level.

The function of the MRDY input is essentially the same as previously described. A timing diagram for the circuit is shown in Figure 8. Since the clocks must be stretched while clock E is high and clock Q is low, the output of the 74LS10 NAND gate is only low when E is high, Q is low, and MRDY is low. This allows a low to be clocked through U2a to the clear input of U3a and the preset input of U3b. In this manner, the E and Q clocks are stretched until MRDY rises and is clocked through with the 4X clock. The clocks then proceed normally from there.

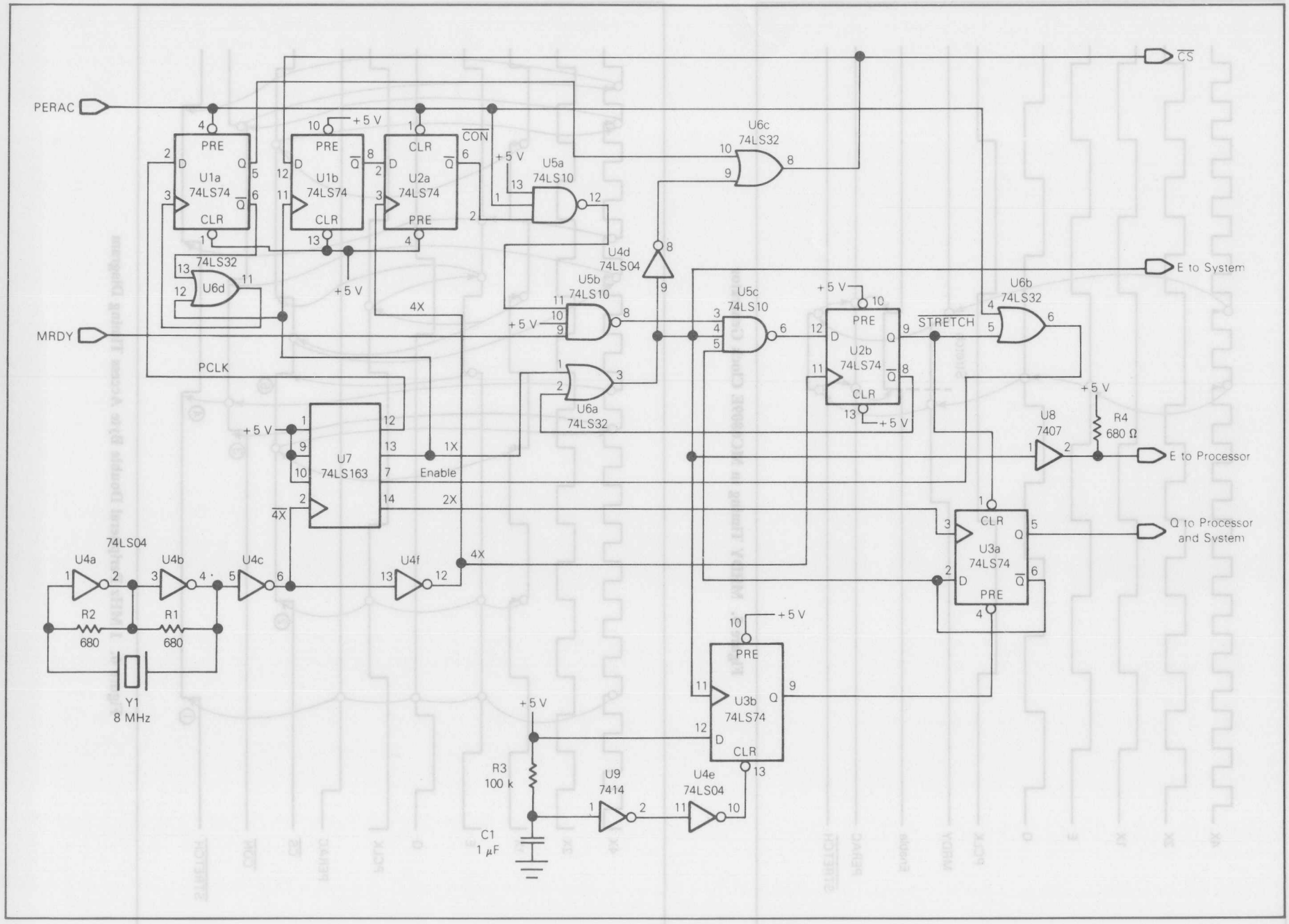


**Figure 4. Clock Generator Circuit for MC6809E**

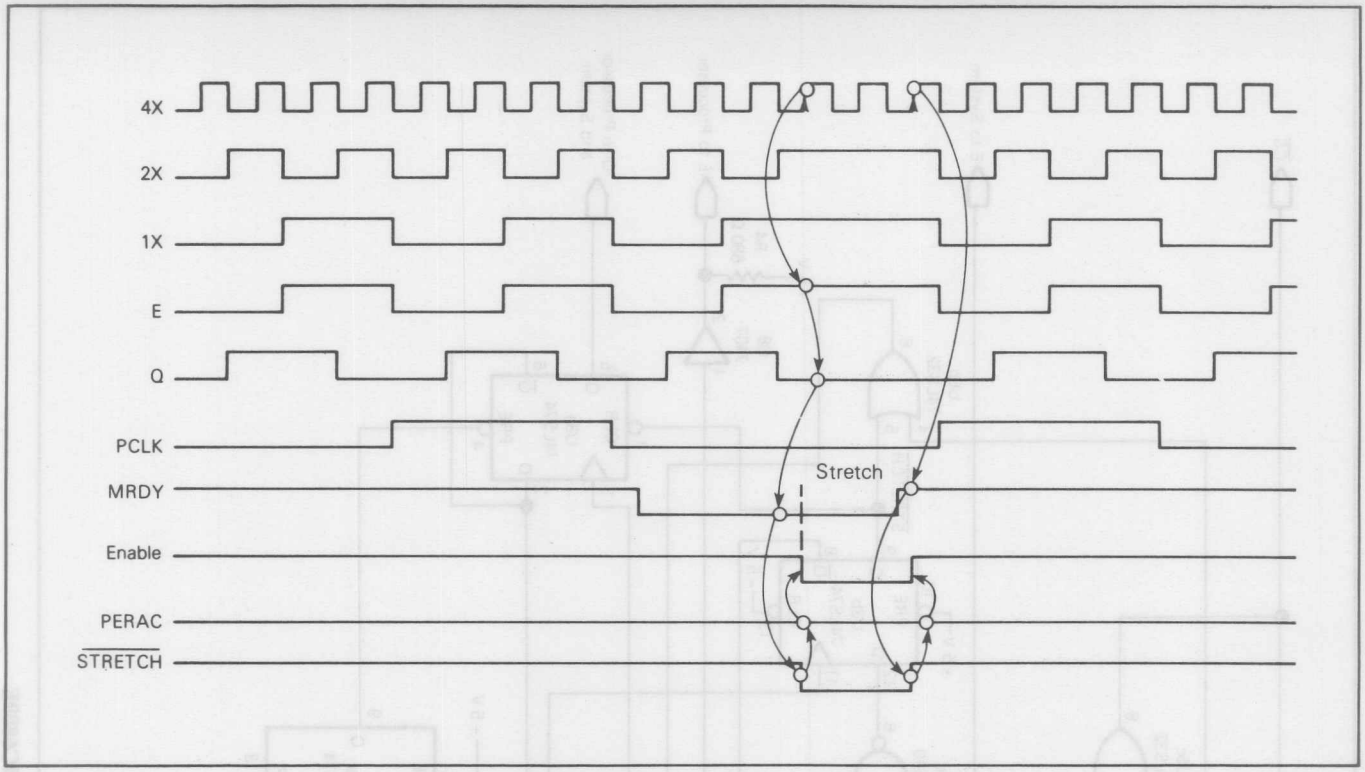


**Figure 5. MRDY Timing in MC6809E Clock Generator**

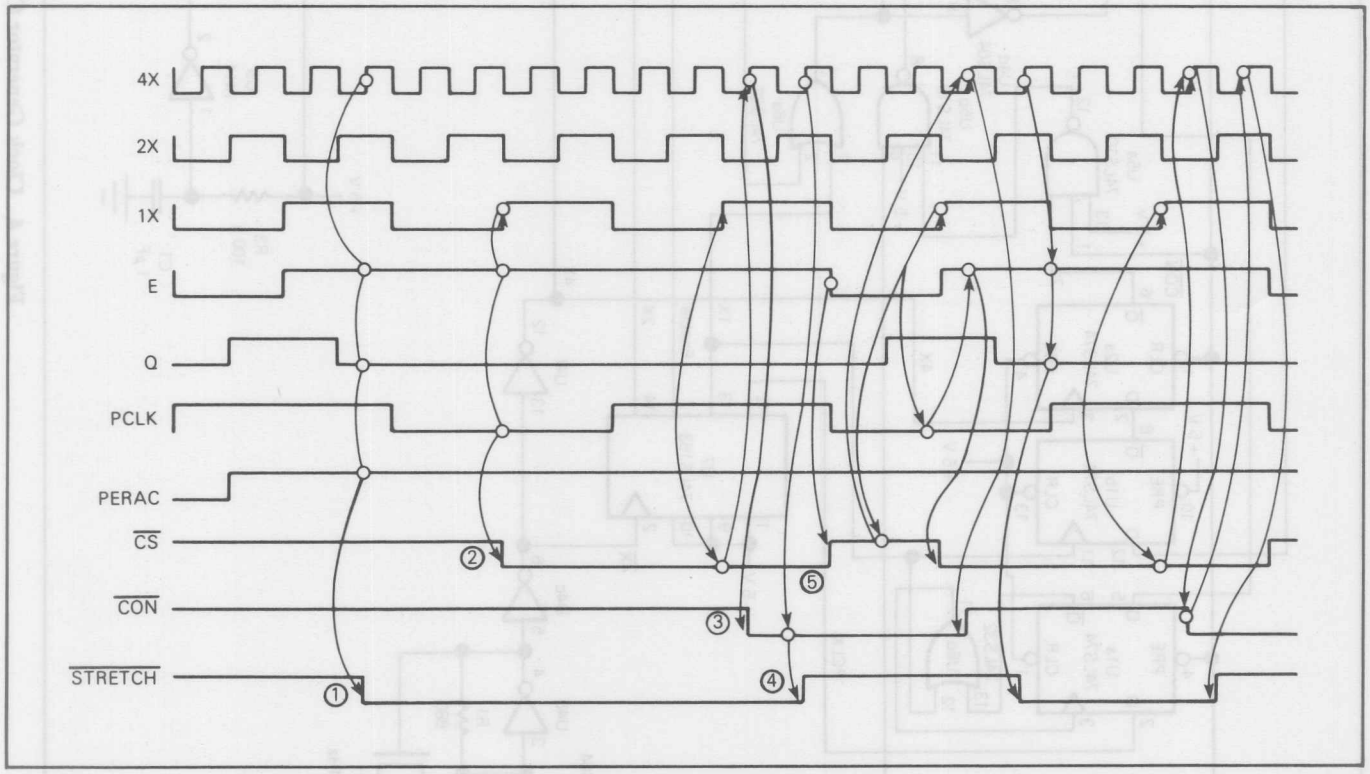


**Figure 6. 1 MHz Peripheral Double Byte Access Timing Diagram**

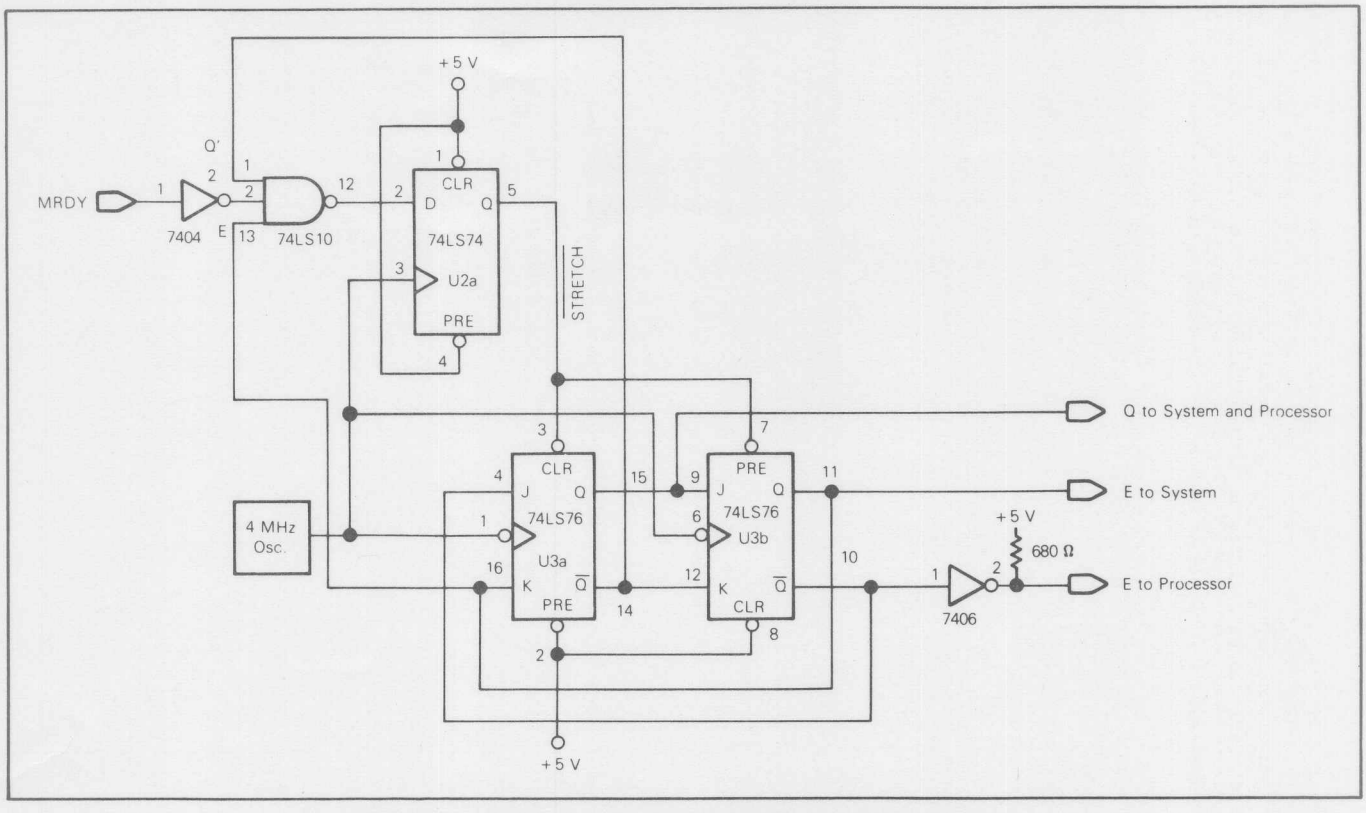


**Figure 7. Clock Generator for MC6809E with MRDY Input**

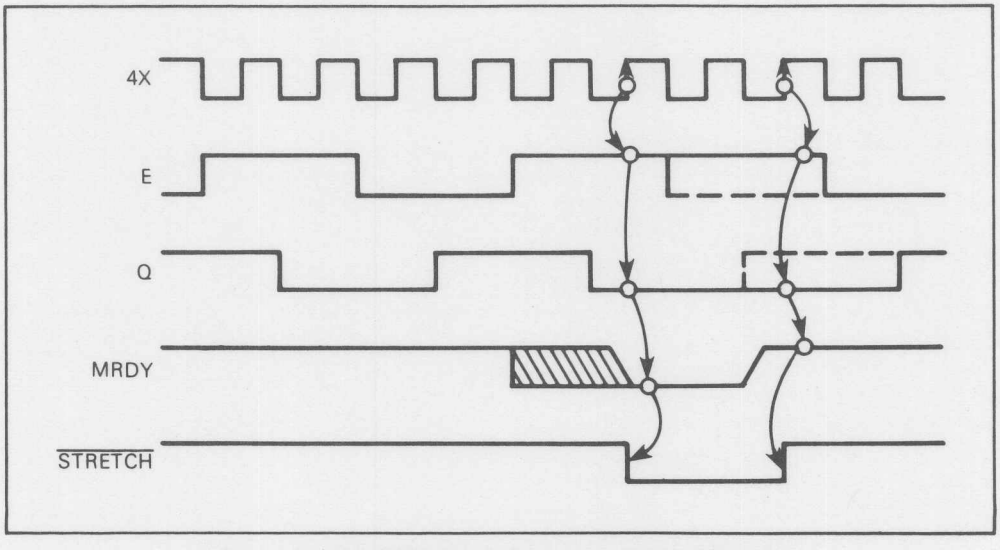


**Figure 8. MC6809E Clock Generator Timing Diagram**

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